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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/788,582	02/16/2001	John Susantha Fernando	9-11-4	8752

7590 12/14/2004

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EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/788,582	FERNANDO ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are presented for examination.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

Specification

3. The disclosure is object to because of the following informalities: the specification must identify any related application/patens by the serial number (not by the Attorney's Docket number and any other number) or patent number, if patented. Please make sure that the related information is up to date. Appropriate correction is required.

4. Claims 1-23 and are rejected under 35 U.S.C. 102(b) as being anticipated by Tateishi (Tateishi), U.S. patent no. 5,539,590.

As per claim 1, Tateishi teaches the invention comprising:

adjusting a voltage level of the control signal [STS, fig. 4] from a previous time interval to indicate a first signal state [change of floppy status – from loaded to unloaded or unloaded to loaded, col. 7, lines 30 – 43, col. 8, lines 49 – 50]; and

maintaining said voltage level of said control signal from the previous time interval to indicate a second signal state [no change of the floppy status].

Specifically, the control signal STS is inputted to the delay FF [DFF] and the EXCLUSIVE-OR gate EX1 [fig. 3]. The output of DFF is connected to the other input of

EX1. When there is no change of the floppy status[1], the two inputs of the EX1 are either both 1 or 0 and the output of EX1 is 0 indicating a second signal state – no change of the floppy status[2]. Where there is a change of floppy status[3], the two inputs of the EX1 are 1 or 0 respectively and the output of EX1 is 1 indicating a first signal state – change of floppy status [col. 7, lines 16 – col. 8 line 51, col. 12, lines 31 – 38].

As per claim 2, Tateishi teaches the step of maintaining said voltage level from the previous time interval using a memory element [DFF, fig. 3; col. 6, lines 11-20].

As per claim 3, Tateishi teaches the step of ensuring that only a single node connected to said bus can assert said control signal in a given time interval [fig. 4; col. 7, lines 30-43].

As per claim 4, Tateishi teaches that bus is on a system-on-chip [fig. 3; col. 4, lines 62-64].

As per claim 5, Tateishi teaches that bus is on a printed circuit board [fig. 3; col. 4, lines 62-64].

As per claim 6, Tateishi teaches of adjust step further comprising the step of transitioning from a first voltage level to a second voltage level [col. 7, lines 30-43].

As per claim 7, Tateishi teaches of adjusting step further comprising the step of applying a high logic level to an exclusive-OR gate with said voltage level from the

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[1] When the floppy is in the floppy drive, the STS signal is high. The signal STS is maintained at the high level as long as the floppy is in the floppy drive. When the floppy is not in the floppy drive, the STS signal is low. The signal STS is maintained at the low level as long as the floppy is not in the floppy drive. [see fig. 4].
[2] The floppy is either continuously inside or outside the floppy drive.
[3] The STS signal changes from either high to low or low to high depending upon whether the floppy is unloaded or loaded into the floppy drive.

previous time interval to determine the signal level to be asserted in the current time interval [fig. 3, col. 7, lines 30-43].

As to claims 8-15 are written in means plus function and contained the same limitations as claims 1-7, therefore same rejection is applied.

As to claims 16-23 basically are the corresponding elements that are carried out the method of operating step in claims 1-7. Accordingly, claims 16-23 are rejected for the same reason as set forth for claims 1-7.

5. Applicant's arguments filed on 10/4/2004 have been fully considered but are moot in view of new ground(s) of rejection.

6. In the remarks, applicants argued in substance that in **Gulick** system does not disclose or suggest adjusting a voltage level of said control signal from a previous time interval to indicate a first signal state.

7. The examiner respectfully traverses. In **Tateishi** system teaches of adjusting a voltage level of said control signal from a previous time interval to indicate a first signal state [col. 7, 30-43]. Also see rejection above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chun Cao

Dec. 8, 2004